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EXAMINER	
AUVE, GLENN ALLEN	
ART UNIT	**PAPER NUMBER**
2181	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/804,224	GREEFF ET AL.	
	Examiner	Art Unit	
	Glenn A. Auve	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 29,51, and 76 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 29,52, and 76 include the limitation that the first data bus is a multidrop bus, however such subject matter is not described in the specification at all. In fact applicant's invention appears to be a system which replaces a multidrop bus architecture with the stubless bus as is claimed in claims 30 and 52 and is described throughout the specification. Because the specification lacks any description of a multidrop bus system included in applicant's invention it would require undue experimentation by one of ordinary skill in the art to make and/or use applicant's invention in a system using such a multidrop bus.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-27,30-49,52-75, and 77 are rejected under 35 U.S.C. 102(e) as being anticipated by Halbert et al., U.S. Pat. No. 6,625,687 B1.

As per claim 1, Halbert et al. (Halbert) shows a first receiver/driver pair coupled to a first segment of a first bus the receiver/driver pair configured to receive data on the first segment using the receiver and place data on the segment using the driver; a second receiver/driver pair coupled to a second segment of the first bus the receiver/driver pair configured to receive data on the second segment using the receiver and place data on the segment using the driver; and a selector circuit connected to the first and second receiver/driver pairs to selectively operate the receiver/driver pairs according to a selection signal such that in a first mode the first receiver/driver pair passes data between the first bus segment and an I/O device and in a second mode the first and second receiver/driver pairs pass data between adjacent bus segments and bypass the I/O device (at least in fig.5 and the accompanying discussion in cols. 5-7, wherein the isolation circuit 510 contains the driver/receiver pairs and the selection circuit for passing data between the bus segments 550 and 570 in the second mode claimed by applicant or between one of the segments and the memory devices 560 or the bus 502 which are the I/O device claimed by applicant). Halbert shows all of the elements recited in claim 1.

As for claim 2, the argument for claim 1 applies. Halbert also shows a selection signal operates the selection circuit and when the signal selects the selector circuit the first and second receiver/driver pairs operate in the first operating mode (at least in col.6 which describes that the address/command signals from the memory controller are used to control the circuit in order to either direct data to the next bus segment or to a memory device in the module). Halbert shows all of the elements recited in claim 2.

As for claim 3, the argument for claim 1 applies. Halbert also shows a selection signal operates the selection circuit and when the signal does not select the selector circuit the first

and second receiver/driver pairs operate in the second operating mode (at least in col.6 which describes that the address/command signals from the memory controller are used to control the circuit in order to either direct data to the next bus segment or to a memory device in the module). Halbert shows all of the elements recited in claim 3.

As for claim 4, the argument for claim 1 applies. Halbert also shows a selection signal operates the selection circuit and when the signal selects the selector circuit the second receiver/driver pair is deactivated to permit point to point data communication using the first receiver/driver pair between the I/O device and another device connected to the first data bus (at least in col.6 which describes that the address/command signals from the memory controller are used to control the circuit in order to either direct data to the next bus segment or to a memory device in the module). Halbert shows all of the elements recited in claim 4.

As for claim 5, the argument for claim 1 applies. Halbert also shows that the first and second receiver/driver pairs are located on a same integrated circuit as a memory device (as above, fig. 5 and cols. 5-7). Halbert shows all of the elements recited in claim 5.

As for claim 6, the argument for claim 1 applies. Halbert also shows that the first and second receiver/driver pairs are located on a memory module (fig.5). Halbert shows all of the elements recited in claim 6.

As for claim 7, the argument for claim 1 applies. Halbert also shows that the I/O device comprises a memory device (560). Halbert shows all of the elements recited in claim 7.

As for claim 8, the argument for claim 1 applies. Halbert also shows that the I/O device comprises a second data bus (502). Halbert shows all of the elements recited in claim 8.

As per claim 9, Halbert shows a first receiver/driver pair coupled to a first segment of a first bus the r ceiver/driver pair configured to receive data on the first segment using the receiver and place data on the segment using the driver; a second receiver/driver pair coupled

to a second segment of the first bus the receiver/driver pair configured to receive data on the second segment using the receiver and place data on the segment using the driver; and an interface circuit connected to the first and second receiver/driver pairs and a second data bus wherein the interface circuit is configured to receive data from the first receiver and selectively place the data on the second data bus and receive data on the second data bus and selectively place the data on the first data bus (at least in fig.5 and the accompanying discussion in cols. 5-7, wherein the isolation circuit 510 contains the driver/receiver pairs and the interface circuit for passing data between the bus segments 550 and 570 or between one of the segments and the second bus 502). Halbert shows all of the elements recited in claim 9.

As for claim 10, the argument for claim 9 applies. Halbert also shows that the interface circuit selects data for receipt from the first and second data buses according to a selection signal on a command and address bus (col.6). Halbert shows all of the elements recited in claim 10.

As for claim 11, the argument for claim 9 applies. Halbert also shows that the interface circuit is configured to receive a selection signal and the interface selectively deactivates the second receiver/driver pair according to the selection signal (at least in col.6 which describes that the address/command signals from the memory controller are used to control the circuit in order to either direct data to the next bus segment or to a memory device in the module). Halbert shows all of the elements recited in claim 11.

As for claim 12, the argument for claim 11 applies. Halbert also shows that the interface deactivates the second pair when the selection signal instructs to interface circuit to transfer data between the first and second buses (at least in col.6 which describes that the address/command signals from the memory controller are used to control the circuit in order to

either direct data to the next bus segment or to a memory device in the module via the second bus 502). Halbert shows all of the elements recited in claim 12.

As for claim 13, the argument for claim 11 applies. Halbert also shows that the interface circuit is connected in a point to point data connection with another device connected to the first data bus when the second pair is deactivated (at least in col.6 which describes that the address/command signals from the memory controller are used to control the circuit in order to either direct data to the next bus segment or to a memory device in the module in a point to point connection). Halbert shows all of the elements recited in claim 13.

As for claim 14, the argument for claim 11 applies. Halbert also shows that the selection signal is received on a command and address bus (col.6). Halbert shows all of the elements recited in claim 14.

As for claim 15, the argument for claim 9 applies. Halbert also shows that the first pair is coupled to the first segment by a first set of I/O pins and the second pair is connected to the second segment by a second set of I/O pins (501 and 503). Halbert shows all of the elements recited in claim 15.

As for claims 16 and 17, the argument for claim 9 applies. Halbert also shows that the interface circuit further comprises at least one multiplexer and a demultiplexer that perform a data rate conversion between the first and second buses (540). Halbert shows all of the elements recited in claims 16 and 17.

As for claim 18, the argument for claim 9 applies. Halbert also shows that the interface circuit further comprises at least one or a coder and a decoder that performs at least one of data encoding and data decoding conversion between the first and second buses (col.7 which describes how the data is transferred between the bus segments of the first bus and the second

bus in such a way that the data is converted into a usable form by the side which is receiving the data). Halbert shows all of the elements recited in claim 18.

As for claim 19, the argument for claim 9 applies. Halbert also shows a voltage converter that performs voltage level conversion between the buses (530). Halbert shows all of the elements recited in claim 19.

As for claim 20, the argument for claim 9 applies. Halbert also shows that the first bus includes a first number of data paths and the second bus includes a second number of paths and the first number is less than the second number (col.7, line 42 – col.8, line 13). Halbert shows all of the elements recited in claim 20.

As for claim 21, the argument for claim 9 applies. Halbert also shows that the second bus is connected to at least one memory device (560). Halbert shows all of the elements recited in claim 21.

As for claim 22, the argument for claim 9 applies. Halbert also shows that the first data bus is connected to a memory controller (111). Halbert shows all of the elements recited in claim 22.

As for claim 23, the argument for claim 9 applies. Halbert also shows that the first bus is connected to a processor (101). Halbert shows all of the elements recited in claim 23.

As for claim 24, the argument for claim 9 applies. Halbert also shows that the first bus operates at a first rate faster than a second rate at which the second bus operates (cols. 6-8). Halbert shows all of the elements recited in claim 24.

As for claim 25, the argument for claim 9 applies. Halbert also shows that the first bus operates at a voltage level less than a second voltage level at which the second bus operates (cols. 6-7). Halbert shows all of the elements recited in claim 25.

As for claim 26, the argument for claim 9 applies. Halbert also shows that the first bus transmits digital signals (inherent in the operation of modern computer systems). Halbert shows all of the elements recited in claim 26.

As for claim 27, the argument for claim 9 applies. Halbert also shows that the first bus transmits digital signals (inherent in the operation of modern computer systems). Halbert shows all of the elements recited in claim 27.

As for claim 30, the argument for claim 9 applies. Halbert also shows that the first bus is substantially stubless (col. 6, lines 44-65). Halbert shows all of the elements recited in claim 30.

As per claim 31, Halbert shows at least one memory device (560); and a data transfer interface connected to a first data bus (550) and to the at least one memory device by a second data bus (502), the interface comprising a first receiver/driver pair coupled to a first segment of a first bus the receiver/driver pair configured to receive data on the first segment using the receiver and place data on the segment using the driver; a second receiver/driver pair coupled to a second segment of the first bus the receiver/driver pair configured to receive data on the second segment using the receiver and place data on the segment using the driver; and an interface circuit connected to the first and second receiver/driver pairs and a second data bus wherein the interface circuit is configured to receive data from the first receiver and selectively place the data on the second data bus and receive data on the second data bus and selectively place the data on the first data bus (at least in fig.5 and the accompanying discussion in cols. 5-7, wherein the isolation circuit 510 contains the driver/receiver pairs and the interface circuit for passing data between the bus segments 550 and 570 or between one of the segments and the second bus 502). Halbert shows all of the elements recited in claim 31.

As for claim 32, the argument for claim 31 applies. Halbert also shows that the interface circuit selects data for transfer between the first and second data buses according to a selection

signal on a command and address bus (col.6). Halbert shows all of the elements recited in claim 32.

As for claim 33, the argument for claim 31 applies. Halbert also shows that the interface circuit is configured to receive a selection signal and the interface selectively deactivates the second receiver/driver pair according to the selection signal (at least in col.6 which describes that the address/command signals from the memory controller are used to control the circuit in order to either direct data to the next bus segment or to a memory device in the module). Halbert shows all of the elements recited in claim 33.

As for claim 34, the argument for claim 33 applies. Halbert also shows that the interface deactivates the second pair when the selection signal instructs to interface circuit to transfer data between the first and second buses (at least in col.6 which describes that the address/command signals from the memory controller are used to control the circuit in order to either direct data to the next bus segment or to a memory device in the module via the second bus 502). Halbert shows all of the elements recited in claim 34.

As for claim 35, the argument for claim 33 applies. Halbert also shows that the interface circuit is connected in a point to point data connection with another device connected to the first data bus when the second pair is deactivated (at least in col.6 which describes that the address/command signals from the memory controller are used to control the circuit in order to either direct data to the next bus segment or to a memory device in the module in a point to point connection). Halbert shows all of the elements recited in claim 35.

As for claim 36, the argument for claim 33 applies. Halbert also shows that the selection signal is received on a command and address bus (col.6). Halbert shows all of the elements recited in claim 36.

As for claim 37, the argument for claim 31 applies. Halbert also shows that the first pair is coupled to the first segment by a first set of I/O pins and the second pair is connected to the second segment by a second set of I/O pins (501 and 503). Halbert shows all of the elements recited in claim 37.

As for claims 38 and 39, the argument for claim 31 applies. Halbert also shows that the interface circuit further comprises at least one multiplexer and a demultiplexer that perform a data rate conversion between the first and second buses (540). Halbert shows all of the elements recited in claims 38 and 39.

As for claim 40, the argument for claim 31 applies. Halbert also shows that the interface circuit further comprises at least one or a coder and a decoder that performs at least one of data encoding and data decoding conversion between the first and second buses (col.7 which describes how the data is transferred between the bus segments of the first bus and the second bus in such a way that the data is converted into a usable form by the side which is receiving the data). Halbert shows all of the elements recited in claim 40.

As for claim 41, the argument for claim 31 applies. Halbert also shows a voltage converter that performs voltage level conversion between the buses (530). Halbert shows all of the elements recited in claim 41.

As for claim 42 the argument for claim 31 applies. Halbert also shows that the first bus includes a first number of data paths and the second bus includes a second number of paths and the first number is less than the second number (col.7, line 42 – col.8, line 13). Halbert shows all of the elements recited in claim 42.

As for claim 43, the argument for claim 31 applies. Halbert also shows that the second bus is connected to at least one memory device (560). Halbert shows all of the elements recited in claim 43.

As for claim 44, the argument for claim 31 applies. Halbert also shows that the first data bus is connected to a memory controller (111). Halbert shows all of the elements recited in claim 44.

As for claim 45, the argument for claim 31 applies. Halbert also shows that the first bus is connected to a processor (101). Halbert shows all of the elements recited in claim 45.

As for claim 46, the argument for claim 31 applies. Halbert also shows that the first bus operates at a first rate faster than a second rate at which the second bus operates (cols. 6-8). Halbert shows all of the elements recited in claim 46.

As for claim 47, the argument for claim 31 applies. Halbert also shows that the first bus operates at a voltage level less than a second voltage level at which the second bus operates (cols. 6-7). Halbert shows all of the elements recited in claim 47.

As for claim 48, the argument for claim 31 applies. Halbert also shows that the first bus transmits digital signals (inherent in the operation of modern computer systems). Halbert shows all of the elements recited in claim 48.

As for claim 49, the argument for claim 31 applies. Halbert also shows that the first bus transmits digital signals (inherent in the operation of modern computer systems). Halbert shows all of the elements recited in claim 49.

As for claim 52, the argument for claim 31 applies. Halbert also shows that the first bus is substantially stubless (col. 6, lines 44-65). Halbert shows all of the elements recited in claim 52.

As per claim 53, Halbert shows a first bus having first and second segments (550,570); a controller connected to place data on and receive data from the first bus (111); a processor coupled to the controller (101); and a data transfer interface comprising a first receiver/driver pair coupled to a first segment of a first bus the receiver/driver pair configured to r ceive data on

the first segment using the receiver and place data on the segment using the driver; a second receiver/driver pair coupled to a second segment of the first bus the receiver/driver pair configured to receive data on the second segment using the receiver and place data on the segment using the driver; and an interface circuit connected to the first and second receiver/driver pairs and a second data bus wherein the interface circuit is configured to receive data from the first receiver and selectively place the data on the second data bus and receive data on the second data bus and selectively place the data on the first data bus (at least in fig.5 and the accompanying discussion in cols. 5-7, wherein the isolation circuit 510 contains the driver/receiver pairs and the interface circuit for passing data between the bus segments 550 and 570 or between one of the segments and the second bus 502). Halbert shows all of the elements recited in claim 53.

As per claim 54, Halbert shows a processor (101); at least on memory subsystem connected to the processor (as in fig.1,113); and a bus (550) coupled to each of a controller and at least one memory subsystem interface circuit whereby the interface circuit (500) couples at least one memory device (560) to said bus (550), the interface comprising a circuit for receiving data from the bus and converting it to data which can be processed by the memory device and for receiving data from the memory device and converting it to data which can be transmitted on the bus (cols. 5-7); and wherein the at least one memory subsystem interface circuit includes first and second receiver/driver pairs connected to the first and second segments of the bus (in the isolation circuit 510 as noted previously). Halbert shows all of the elements recited in claim 54.

As for claim 55, the argument for claim 54 applies. Halbert also shows that the controller resides on the same circuit board as the processor (cols. 5-7). Halbert shows all of the elements recited in claim 55.

As for claim 56, the argument for claim 54 applies. Halbert also shows that the controller is integrated into the processor (cols. 5-7). Halbert shows all of the elements recited in claim 56.

As per claim 57, Halbert shows receiving data at first and second receivers coupled to first and second segments of a first data bus; and driving data using first and second drivers coupled to the first and second segments according to a selection signal such that in a first mode a first receiver/driver pair passes signals between the first segment and an I/O device, and in a second mode the receiver/driver pairs pass signals between their bus segments and bypass the I/O device (at least in fig.5 and the accompanying discussion in cols. 5-7, wherein the isolation circuit 510 contains the driver/receiver pairs and the selection circuit for passing data between the bus segments 550 and 570 in the second mode claimed by applicant or between one of the segments and the memory devices 560 or the bus 502 which are the I/O device claimed by applicant). Halbert shows all of the steps recited in claim 57.

As for claim 58, the argument for claim 57 applies. Halbert also shows that the I/O device comprises a memory device (560). Halbert shows all of the steps recited in claim 58.

As for claim 59, the argument for claim 57 applies. Halbert also shows that the I/O device comprises a second data bus (502). Halbert shows all of the steps recited in claim 59.

As per claim 60, Halbert shows connecting an interface circuit (500) having first and second receiver/driver pairs to first and second segments of a first data bus (550,570) that operates at a first data rate; connecting the interface circuit to a second data bus (502) that operates at a second data rate; receiving and transmitting data on the first bus using the receiver/driver pairs; receiving and transmitting data on the second bus; selectively placing data received from the first bus segment on the second bus segment; selectively placing data received from the second bus segment on the first bus segment; and selectively converting data received from one of the first or second data buses for use on the other bus (as noted above in

cols. 5-7, wherein the data can be sent to and from the bus segments or converted for use by the memory devices 560). Halbert shows all of the steps recited in claim 60.

As for claim 61, the argument for claim 60 applies. Halbert also shows that the selective conversion is performed according to a selection signal (cols. 5-7, the commands and addresses provided on the command and address bus from the memory controller are used to control the interface and select how the data should be routed). Halbert shows all of the steps recited in claim 61.

As for claim 62, the argument for claim 61 applies. Halbert also shows that the conversion is performed when the interface circuit is selected for operation by the select signal (cols. 5-7, the commands and addresses provided on the command and address bus from the memory controller are used to control the interface and select how the data should be routed). Halbert shows all of the steps recited in claim 62.

As for claim 63, the argument for claim 61 applies. Halbert also shows that the conversion is not performed when the interface circuit is not selected for operation by the select signal (cols. 5-7, the commands and addresses provided on the command and address bus from the memory controller are used to control the interface and select how the data should be routed). Halbert shows all of the steps recited in claim 63.

As for claim 64, the argument for claim 61 applies. Halbert also shows that the second receiver/driver pair is deactivated when the interface circuit is selected for operation by the selection signal (cols. 5-7, the commands and addresses provided on the command and address bus from the memory controller are used to control the interface and select how the data should be routed, and the data are not routed to the other bus segments when they are to be sent to the memory devices on the memory module). Halbert shows all of the steps recited in claim 64.

As for claim 65, the argument for claim 61 applies. Halbert also shows that when the interface circuit is not selected for operation by the signal, data on the first segment is passed to the second segment and data on the second segment is passed to the first segment (cols. 5-7, the commands and addresses provided on the command and address bus from the memory controller are used to control the interface and select how the data should be routed, and the data are routed between the bus segments when they are not to be sent to the memory devices on the memory module). Halbert shows all of the steps recited in claim 65.

As for claim 66, the argument for claim 60 applies. Halbert also shows that the first data rate is faster than the second (cols. 6-7). Halbert shows all of the steps recited in claim 66.

As for claim 67, the argument for claim 60 applies. Halbert also shows converting data between the data rate of the first bus and the data rate of the second bus (cols. 6-7). Halbert shows all of the steps recited in claim 67.

As for claim 68, the argument for claim 60 applies. Halbert also shows converting data between a first encoding on the first bus and a second encoding on the second bus (cols. 6-7). Halbert shows all of the steps recited in claim 68.

As for claim 69, the argument for claim 60 applies. Halbert also shows converting data between a first voltage level on the first bus and a second voltage level on the second bus (cols. 5-7, voltage translator 530). Halbert shows all of the steps recited in claim 69.

As for claim 70, the argument for claim 69 applies. Halbert also shows that the first voltage is less than the second voltage (cols. 5-7, voltage translator 530). Halbert shows all of the steps recited in claim 70.

As for claim 71, the argument for claim 60 applies. Halbert also shows that the first data bus uses a first width different from the width of the second bus (cols. 5-7, mux/demux 540). Halbert shows all of the steps recited in claim 71.

As for claim 72, the argument for claim 71 applies. Halbert also shows that the first width is less than the second width (cols. 5-7, mux/demux 540). Halbert shows all of the steps recited in claim 72.

As for claim 73, the argument for claim 60 applies. Halbert also shows that devices of a first technology communicate with the interface circuit using the first bus and devices of a second technology communicate with the interface using the second bus (figs.1 and 5). Halbert shows all of the steps recited in claim 73.

As for claim 74, the argument for claim 73 applies. Halbert also shows that the devices of the first technology include at least one processor (101). Halbert shows all of the steps recited in claim 74.

As for claim 75, the argument for claim 73 applies. Halbert also shows that the devices of the second technology include at least one memory device (560). Halbert shows all of the steps recited in claim 75.

As for claim 77, the argument for claim 60 applies. Halbert also shows that the first bus is substantially stubless (col. 6, lines 44-65). Halbert shows all of the steps recited in claim 77.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 28, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert in view of Official Notice.

As for claims 28 and 50, the arguments above for claims 9 and 31, respectively apply. Halbert does not specifically show the use of radio frequency (RF) signals to transmit data on the first bus. However, Official Notice is taken that the use of RF signals to transmit data is very well known in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to communicate data using RF signals as is well known in the system of Halbert in order to eliminate wire lines and allow for operation over a distance or to reduce wiring costs.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The other cited references also show memory repeater systems that allow for stubless operation and either pass the data to memory devices attached to a module or pass the signals on to the next bus segment to be used by another module farther down the line.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (703) 305-9638. The examiner can normally be reached on M-Th 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephon are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Glenn A. Auve
Primary Examiner
Art Unit 2181

gaa
September 25, 2003